

**REMARKS**

Reconsideration and allowance in view of the foregoing amendments and the following remarks are respectfully requested.

Claims 1, 4 and 11 have been amended. Claims 1-17 are pending in this application.

Claims 1-17 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 5,416,783 granted to Broseghini et al. Claims 1-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,321,320 granted to Fleischman et al. Applicant traverses the rejections for the following reasons.

Amended claim 1 recites, in part, a code ROM for storing and outputting data in response to an address and a read enabled signal, a first encryption means for encrypting the data outputted from the code ROM, a second encryption means for encrypting a test enable signal based on key data to generate a read enabled signal, and an output means for dumping out the encrypted data outputted from the first encryption means in response to the read enable signal outputted from the second encryption means. Applicant submits that the references cited by the Examiner fail to disclose or suggest all of the features of the claimed invention.

While Broseghini et al. describes a data compression method, the reference fails to disclose or suggest the code ROM and the second encryption means and the output means of the claimed invention. Applicant has carefully reviewed the passages in Broseghini et al. pointed out by the Examiner, columns 11-15, but Applicant could not find any relevant passages which describe the code ROM for storing and outputting the data in response to an address and read enabled signal, the second encryption means for encrypting a test enable signal based on key data to generate a read enable signal, and the output means for dumping out the encrypted data outputted from the first encryption means in response to the read enabled signal outputted from the second encryption means. The Examiner is cordially

invited to point out any other particular passages which describe or teach these elements of claim 1.

Similarly, Fleischman et al. also fails to disclose or suggest most of the elements of the claimed invention. While Fleischman et al. discloses MISR compressing data sequence on a bus into a single "signature" through a process of XORing and shifting new data with current data (column 6, lines 55-59), Fleischman et al. fails to disclose at least a second encryption means for encrypting a test enable signal based on key data to generate a read enable signal and an output means for dumping out the encrypted data outputted from a first encryption means in response to the read enabled signal outputted from the second encryption means.

Claim 11 recites similar elements, but in detailed circuit level, as claim 1. As a result, Broseghini et al. and Fleischman et al. also fail to disclose or suggest at least the comparison unit for outputting a read enable signal by comparing value outputted from MISR unit with an expected value, and an output means for dumping the code ROM data in response to the read enable signal.


Therefore, claims 1 and 11 and their dependent claims 2-10 and 12-17 are not anticipated by Broseghini et al. under 35 U.S.C. §102(b) or by Fleischman et al. under 35 U.S.C. §102(e).

The prior art made of record and not relied upon is noted.

All objections and rejections having been addressed, it is respectfully submitted that claims 1-17 are now in condition for allowance and a notice to that effect is earnestly solicited. If any issues remain to be resolved, the Examiner is cordially invited to telephone the undersigned attorney at the number listed below.

Respectfully submitted,

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